Application No.: 10/705,946

REMARKS

Claims 1-25 are active and pending in the present application; all of which stand rejected under 35 U.S.C. § 103 as unpatentable over Van Hook (US Patent No. 6,266,758) in view of Motorola MC68030 users manual. In response, the following remarks are provided and new claims 26-55 are presented.

Support for Claims 26-55

New claims 26-55 are fully supported by the present specification. Support for specific claim elements is identified below by citing to the present specification as published (United States Pub. No. US 2004/0103266).

Regarding claim 26, the recited programmable processor comprising in part "an instruction path; a data path; a plurality of registers operable to receive and store data from the data path and communicate the stored data to the data path" is described at Figure 1 and paragraphs 0078 – 0080.

Regarding claim 26, the recited programmable processor further comprising in part "execution unit coupled to the instruction path and the data path and operable to decode and execute instructions received from the instruction path, wherein in response to decoding a single group shift right instruction specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register, the execution unit is operable to: (i) for each of the plurality of data elements in the operand register, shift a subfield of the data element towards the least significant bit by the shift

amount and fill a shift amount number of most significant bits with the sign bit of the respective data element to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0229 and 0233.

Regarding claim 27, the recited claim feature "wherein the execution unit is operable to execute group shift right instructions on 16-bit, 32-bit and 64-bit signed integer data" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0031, 0229 and 0233.

Regarding claim 28, the recited claim feature "wherein the operand register is a 128-bit register and the destination register is a 128-bit register" is described at Figures 43A-C and 43H-J, and paragraphs 0229 and 0233.

Regarding claim 29, the recited claim feature "wherein the shift amount is contained in an immediate field of the instruction" is described at Figures 43H-J, and paragraph 0233.

Regarding claim 30, the recited claim feature "wherein the shift amount is contained in a register specified by the instruction" is described at Figures 43A-C and paragraph 0229.

Regarding claim 31, the recited programmable processor comprising in part "an instruction path; a data path; a plurality of registers operable to receive and store data from the data path and communicate the stored data to the data path" is described at Figure 1 and paragraphs 0078 – 0080.

Regarding claim 31, the recited programmable processor further comprising in part "an execution unit coupled to the instruction path and the data path and operable to decode and execute instructions received from the instruction path, wherein in response to decoding a single

group shift right instruction specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register, the execution unit is operable to: (i) for each of the plurality of data elements in the operand register, shift a subfield of the data element towards the least significant bit by the shift amount and fill a shift amount number of most significant bits with zeros to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0229 and 0233.

Regarding claim 32, the recited claim feature "wherein the execution unit is operable to execute group shift right instructions on 16-bit, 32-bit and 64-bit unsigned integer data" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081,0229 and 0233.

Regarding claim 33, the recited claim feature "wherein the operand register is a 128-bit register and the destination register is a 128-bit register" is described at Figures 43A-C and 43H-J, and paragraphs 0229 and 0233.

Regarding claim 34, the recited claim feature "wherein the shift amount is contained in an immediate field of the instruction" is described at Figures 43H-J, and paragraph 0233.

Regarding claim 35, the recited claim feature "wherein the shift amount is contained in a register specified by the instruction." is described at Figures 43A-C and paragraph 0229.

Regarding claim 36, the recited programmable processor comprising in part "an instruction path; a data path; a plurality of registers operable to receive and store data from the

data path and communicate the stored data to the data path" is described at Figure 1 and paragraphs 0078 – 0080.

Regarding claim 36, the recited programmable processor further comprising in part "an execution unit coupled to the instruction path and the data path and operable to decode and execute instructions received from the instruction path, wherein in response to decoding a single group shift left instruction specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register, the execution unit is operable to: (i) for each of the plurality of data elements in the operand register, shift a subfield of the data element towards the most significant bit by the shift amount and fill a shift amount number of least significant bits with the sign bit of the respective data element to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0229 and 0233.

Regarding claim 37, the recited claim feature "wherein the execution unit is operable to execute group shift left instructions on 16-bit, 32-bit and 64-bit signed integer data" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0229 and 0233.

Regarding claim 38, the recited claim feature "wherein the operand register is a 128-bit register and the destination register is a 128-bit register" is described at Figures 43A-C and 43H-J, and paragraphs 0229 and 0233.

Regarding claim 39, the recited claim feature "wherein the shift amount is contained in an immediate field of the instruction" is described at Figures 43H-J, and paragraph 0233.

Regarding claim 40, the recited claim feature "wherein the shift amount is contained in a register specified by the instruction." is described at Figures 43A-C and paragraph 0229.

Regarding claim 41, the recited claim feature of a method for shifting data in a programmable processor comprising "decoding a single group shift right instruction specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register; for each of the plurality of data elements in the operand register, shifting a subfield of the data element towards the least significant bit by the shift amount and fill a shift amount number of most significant bits with the sign bit of the respective data element to produce a second plurality of equal-sized data elements; and providing the second plurality of data elements as a catenated result to the destination register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0229 and 0233.

Regarding claim 42, the recited claim feature "wherein the execution unit is operable to execute group shift right instructions on 16-bit, 32-bit and 64-bit signed integer data" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0229 and 0233.

Regarding claim 43, the recited claim feature "wherein the operand register is a 128-bit register and the destination register is a 128-bit register" is described at Figures 43A-C and 43H-J, and paragraphs 0229 and 0233.

Regarding claim 44, the recited claim feature "wherein the shift amount is contained in an immediate field of the instruction" is described at Figures 43H-J, and paragraph 0233.

Regarding claim 45, the recited claim feature "wherein the shift amount is contained in a register specified by the instruction." is described at Figures 43A-C and paragraph 0229.

Regarding claim 46, the recited claim feature of a method for shifting data in a programmable processor comprising "decoding a single group shift right instruction specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register; for each of the plurality of data elements in the operand register, shifting a subfield of the data element towards the least significant bit by the shift amount and fill a shift amount number of most significant bits with zeros to produce a second plurality of equal-sized data elements; and providing the second plurality of data elements as a catenated result to the destination register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0229 and 0233.

Regarding claim 47, the recited claim feature "wherein the execution unit is operable to execute group shift right instructions on 16-bit, 32-bit and 64-bit unsigned integer data" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0229 and 0233.

Regarding claim 48, the recited claim feature "wherein the operand register is a 128-bit register and the destination register is a 128-bit register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0229 and 0233.

Regarding claim 49, the recited claim feature "wherein the shift amount is contained in an immediate field of the instruction" is described at Figures 43H-J, and paragraph 0233.

Regarding claim 50, the recited claim feature "wherein the shift amount is contained in a register specified by the instruction." is described at Figures 43A-C and paragraph 0229.

Regarding claim 51, the recited claim feature of a method for shifting data in a programmable processor comprising "decoding a single group shift left instruction specifying a

shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register; for each of the plurality of data elements in the operand register, shifting a subfield of the data element towards the most significant bit by the shift amount and fill a shift amount number of least significant bits with the sign bit of the respective data element to produce a second plurality of equal-sized data elements; and providing the second plurality of data elements as a catenated result to the destination register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0229 and 0233.

Regarding claim 52, the recited claim feature "wherein the execution unit is operable to execute group shift left instructions on 16-bit, 32-bit and 64-bit signed integer data" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0229 and 0233.

Regarding claim 53, the recited claim feature "wherein the operand register is a 128-bit register and the destination register is a 128-bit register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0229 and 0233.

Regarding claim 54, the recited claim feature "wherein the shift amount is contained in an immediate field of the instruction" is described at Figures 43H-J, and paragraph 0233.

Regarding claim 55, the recited claim feature "wherein the shift amount is contained in a register specified by the instruction." is described at Figures 43A-C and paragraph 0229.

Rejection under 35 U.S.C. § 103

Regarding the obviousness rejections, the primary Van Hook reference does not qualify as prior art to the pending claims, because the present application claims priority back to the

August 16, 1995, filing date of U.S. Patent No. 5,742,840 (the '840 patent), as indicated by the priority claim, which is hereby reproduced for the convenience of the Examiner:

> "This application is a continuation of U.S. Patent Application No. 09/922,319, filed August 2, 2001, [now U.S. Patent No. 6,725,356 issued on April 20, 2004,] which is a Continuation of U.S. Patent Application No. 09/382,402, filed August 24, 1999, now U.S. Patent No. 6,295,599, which claims the benefit of priority to Provisional Patent Application No. 60/097,635 filed August 24, 1998, and is a continuation-in-part of U.S. Patent Application No. 09/169,963, filed October 13, 1998, now U.S. Patent No. 6,006,318, which is a continuation of U.S. Patent Application No. 08/754,827, filed November 22, 1996 now U.S. Patent No. 5,822,603, which is a divisional of U.S. Patent Application No. 08/516,036, filed August 16, 1995 now U.S. Patent No. 5,742,840."

Support for all the pending claims is found in the disclosure of the `840 patent. Van Hook's filing date was March 5, 1999, more than one year later than the August 15, 1995 filing date of the `840 patent. Therefore, Van Hook is not prior art to the claims of the present application.

As the priority claim states, U.S. Patent 6,295,599 ("the `599 patent" is in the direct chain of priority for the present application. Applicants note that various amendments were made to the specification of the `599 patent for submission as the specification of the present application. However, no new matter was added, since the amendments to the specification were made exclusively by inserting materials from the appendix of the `599 patent ("the '599 appendix"). The '599 appendix is (a) attached as an appendix in microfiche form in the '599 patent, (b) attached in CD-ROM format and incorporated by reference in U.S. Patent Application No. 09/922,319, which is a continuation of the '599 patent and the immediate parent of the present application.

To provide support for the claims and comply with MPEP 608.01(i), amendments were made to the specification of the `599 patent for submission in the present specification, which included adding both text and new Figs. 12 through 49G from the `599 appendix, primarily

related to different embodiments of various instructions that the invention is capable of executing. Many of these specific instructions are illustrated in new Figs. 31A through 47C, which are reproduced directly from the '599 appendix. Text corresponding to Figs. 31A through 47C is derived from the '599 appendix and describes the specific processor instructions set forth in those figures.

Pending claims 1-25 are fully supported by the '840 patent and its appendix ("the '840 appendix"), as well as by the '599 patent and the '599 appendix. Thus, claims 1-25 should be accorded an effectively filing date of August 16, 1995. Support for specific claim elements in both the '840 patent and the '599 patent is provided below.

A programmable processor, as recited in claim 1, is described in the '840 patent at col. 4, lines 2-5 and in the '599 patent at col. 1, lines 56-60 and col. 15 line 9. A data path is described in the '840 patent at col. 4, lines 27-28 and in the '599 patent at col. 5, lines 8-10; and an instruction path is described, for example, in the '840 patent at col. 14, lines 11-26. The recited processor includes an external interface (See Fig. 1, element 118 of the '599 patent). As shown in Fig. 1 of the '599 patent, a cache memory 117 is arranged in communication with a bus interface 118, as recited in claim 1 as well. A register file, as recited, is described in the '840 patent at col. 4, lines 33-35 and in the '599 patent at col. 4, lines 18-19. An execution unit is described in the '840 patent at col. 4, lines 35-38 and in the '599 patent at col. 5, lines 44 and 51-56 with the capability to execute and decode instructions. .

In particular, claim 1 also recites that decoding a single instruction specifying both a shift amount and a register having a register width, the register containing a first plurality of data elements having an elemental width smaller than the register width, the number of data elements in the first plurality of data elements being inversely related to the elemental width, the shift

amount configurable to an amount inclusively between zero and one less than the elemental width, the execution unit is operable to: (i) shift a subfield of each of the first plurality of data elements by the shift amount to produce a second plurality of data elements; and (ii) provide the second plurality of data elements as a catenated result. In the present application, this functionality is described in more detail starting at paragraph [0225]. Exemplary instructions that include this specific functionality are described in the '599 Appendix and the '840 Appendix, for example, and include

(a) G.SHR, G.U.SHR G.SHR.I, G.U.SHR.I (described in the '840 appendix at pages 103-105, 119)

(b) X.SHR, X.SHR.U, X.SHR.I, X.SHR.I.U (described in the '599 appendix at pages 188, 206)

With regard to claim 2, the '840 Appendix, at page 106, explains the result is placed in a register specified by "rc". With regard to claim 3, the description of the instruction at page 106 explains the use of values in the registers and, with regard to claim 4, at page 112, the operation of the instruction having the specified shift amount is described. With regard to claims 5 – 7, the pseudo code, for example, on pages 106-109 with respect to G.SHR and G.U.SHR detail how the specific bits of the instructions and registers are defined and aligned.

With respect to claims 8-10, the table on page 106 (of the '840 Appendix) illustrates instructions utilizing 16, 32, and 128 bits. With respect to claims 11-13, the programmable nature of the claimed processor and the flexibility with which the elemental widths of the different data elements may be specified within an instruction support the specific relative data sizes recited in these claims.

Claims 14-25 recite claim features similar to those recited in claims 1-13 wherein claims 1-13 relate to a programmable processor and claims 14-25 relate to an analogous method for

shifting data in a programmable processor. Accordingly, the support in the '599 Appendix and the '840 Appendix identified with regard to claims 1-13 is also applicable to claims 14-25.

As illustrated, all pending claims are supported by the '840 patent and/or the '840 appendix, and the '599 patent and/or the '599 appendix. That is, all pending claims 1-25 have a priority date back to August 1995, which predates Van Hook. Thus, Van Hook does not qualify as a prior art reference for purposes of the Examiner's obviousness rejection. Therefore, Applicants respectfully request that rejections of claims 1-25 under 35 U.S.C. § 103(a) be withdrawn. Furthermore, the newly added claims 26-55 are also supported by the earlier disclosures and are entitled to a priority date which predates Van Hook.

Accordingly, it is believed that all pending claims are now in condition for allowance. Applicants therefore respectfully request an early and favorable reconsideration and allowance of this application. If there are any outstanding issues which might be resolved by an interview or an Examiner's amendment, the Examiner is invited to call Applicants' representative at the telephone number shown below.

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To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,

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